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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,850	EICHLER ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 26 recites the limitation "the PCI bus" in Lines 4 and 8. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 27 recites the limitation "the PCI bus" in Line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 5, 7, 12, 13, 18, 22, 23, 24, and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Number 6,046,742 to Chari "Chari".

6. In reference to Claim 1, Chari teaches that the adapter card slots are designed to receive PCI cards (See Column 6 Lines 49-59), which are inherently connected to the card slots through a PCI bus; identifying a plurality of slots in the computing device (See Figure 34); identifying at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Figure 34); and identifying an unoccupied PCI slot (See Figure 34). Because information pertaining to the slots is provided by the computer system, no physical inspection of the slots is required.

7. In reference to Claim 6, Chari teaches the limitations as applied to Claim 1 above. Chari further teaches that each slot provides an indication of whether an adapter is present or absent from said slot (See Figure 34). Therefore, the system is able to determine how many slots are unoccupied.

8. In reference to Claim 7, Chari teaches that the adapter card slots are designed to receive PCI cards (See Column 6 Lines 49-59), which are inherently connected to the card slots through a PCI bus; identifying a plurality of slots in the computing device (See Figure 34); identifying at least one PCI device coupled to a PCI bus coupled to the PCI

slot (See Figure 34); and identifying an unoccupied PCI slot (See Figure 34). Because information pertaining to the slots is provided by the computer system, no physical inspection of the slots is required. Chari further teaches an apparatus in retrieving information about PCI slots is an application run on a computer system (See Figures 1, 4, and 7, Column 2 Lines 54-67, and Column 3 Lines 1-9 of Chari), and therefore inherently includes software encoded on a computer readable medium.

9. In reference to Claim 12, Chari teaches the limitations as applied to Claim 7 above. Chari further teaches that each slot provides an indication of whether an adapter is present or absent from said slot (See Figure 34). Therefore, the system is able to determine how many slots are unoccupied.

10. In reference to Claim 13, Chari teaches that the adapter card slots are designed to receive PCI cards (See Column 6 Lines 49-59), which are inherently connected to the card slots through a PCI bus; a memory that is inherently part of the computer system (See Figure 1 and Column 6 Lines 35-48) and operable to store information identifying a plurality of slots in the computing device (See Figure 34); and a processor coupled to the memory (See Figure 1 and Column 6 Lines 35-48) and operable to identify at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Figure 34), and identify an unoccupied PCI slot (See Figure 34). Because information pertaining to the slots is provided by the computer system, no physical inspection of the slots is required.

11. In reference to Claim 18, Chari teaches the limitations as applied to Claim 13 above. Chari further teaches that each slot provides an indication of whether an adapter is present or absent from said slot (See Figure 34). Therefore, the system is able to determine how many slots are unoccupied.

12. In reference to Claim 22, Chari teaches the limitations as applied to Claim 1 above. Chari further teaches generating a list of identified PCI slots associated with the computing device (See Figures 32, 33, and 34).

13. In reference to Claim 24, Chari teaches the limitations as applied to Claim 7 above. Chari further teaches generating a list of identified PCI slots associated with the computing device (See Figures 32, 33, and 34).

14. Claims 1, 6, 7, and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by US Patent Number 6,134,621 to Kelley et al. ("Kelley").

15. In reference to Claim 1, Kelley teaches identifying a plurality of PCI slots in a computing device (See Column 1 Lines 20-21); identifying at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Column 2 Lines 13-28); and identifying an unoccupied PCI slot without requiring physical inspection of the PCI slots (See Column 2 Lines 55-58).

16. In reference to Claim 6, Kelley teaches the limitations as applied to Claim 1 above. Kelley further teaches determining how many identified PCI slots are unoccupied (See Column 3 Lines 16-55). Further, since occupied slots output a PRSNT# signal, any slot not outputting said signal is unoccupied (See Column 2 Lines 55-58).

17. In reference to Claim 7, Kelley teaches identifying a plurality of PCI slots in a computing device (See Column 1 Lines 20-21); identifying at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Column 2 Lines 13-28); and identifying an unoccupied PCI slot without requiring physical inspection of the PCI slots (See Column 2 Lines 55-58). Kelley further teaches that the system can be implemented using microcode (analogous to software encoded on a computer readable medium) (See Column 4 Lines 36-39).

18. In reference to Claim 12, Kelley teaches the limitations as applied to Claim 7 above. Kelley further teaches determining how many identified PCI slots are unoccupied (See Column 3 Lines 16-55). Further, since occupied slots output a PRSNT# signal, any slot not outputting said signal is unoccupied (See Column 2 Lines 55-58).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 2, 5, 8, 11, 14, 17, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chari as applied to Claims 1, 7, and 13 above, and further in view of US Patent Number 6,397,268 to Cepulis ("Cepulis").

21. In reference to Claim 2, Chari teaches the limitations as applied to Claim 1 above. Chari does not teach identifying the bus number and device number for at least one PCI slot using a PCI Interrupt Request Routing Table. Cepulis teaches the use of a PCI Interrupt Request Routing Table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use of Cepulis, resulting in the invention of Claim 2, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a

means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

22. In reference to Claim 5, Chari and Cepulis teach the limitations as applied to Claim 1 above. Chari does not teach comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices. Cepulis teaches comparing the PCI IRQ Routing Table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use and comparison of Cepulis, resulting in the invention of Claim 5, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

23. In reference to Claim 8, Chari teaches the limitations as applied to Claim 7 above. Chari does not teach identifying the bus number and device number for at least one PCI slot using a PCI Interrupt Request Routing Table. Cepulis teaches the use of a

PCI Interrupt Request Routing Table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use of Cepulis, resulting in the invention of Claim 8, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

24. In reference to Claim 11, Chari and Cepulis teach the limitations as applied to Claim 7 above. Chari does not teach comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at least one of the identified PCI devices. Cepulis teaches comparing the PCI IRQ Routing Table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use and comparison of Cepulis, resulting in the invention of Claim 11, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was

loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

25. In reference to Claim 14, Chari teaches the limitations as applied to Claim 13 above. Chari does not teach identifying the bus number and device number for at least one PCI slot using a PCI Interrupt Request Routing Table. Cepulis teaches the use of a PCI Interrupt Request Routing Table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use of Cepulis, resulting in the invention of Claim 14, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

26. In reference to Claim 17, Chari and Cepulis teach the limitations as applied to Claim 13 above. Chari does not teach comparing a bus number and a device number of at least one of the identified PCI slots to a bus number and a device number of at

least one of the identified PCI devices. Cepulis teaches comparing the PCI IRQ Routing Table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use and comparison of Cepulis, resulting in the invention of Claim 17, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

27. In reference to Claim 23, Chari teaches the limitations as applied to Claim 1 above. Chari does not teach identifying at least one PCI device coupled to a PCI bus comprising generating a list of one or more PCI devices coupled to the PCI bus. Cepulis teaches an NVRAM data structure that stores the information about each PCI device in the computer system (analogous to generating a list of one or more PCI devices coupled to the PCI bus) (See Column 5 Lines 54-61).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the NVRAM list of PCI devices coupled to the PCI bus of Cepulis, resulting in the invention of Claim 23, in order to provide a means for storing

the information regarding the presence of a device (See Column 5 Lines 38-42 of Cepulis); provide the information to the computer system faster upon startup (See Column 5 Lines 26-38 of Cepulis); and to provide the device of Chari with a means for determining if a device is present, since Chari does not specifically state how the information is obtained.

28. In reference to Claim 25, Chari teaches the limitations as applied to Claim 7 above. Chari does not teach identifying at least one PCI device coupled to a PCI bus comprising generating a list of one or more PCI devices coupled to the PCI bus. Cepulis teaches an NVRAM data structure that stores the information about each PCI device in the computer system (analogous to generating a list of one or more PCI devices coupled to the PCI bus) (See Column 5 Lines 54-61).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the NVRAM list of PCI devices coupled to the PCI bus of Cepulis, resulting in the invention of Claim 25, in order to provide a means for storing the information regarding the presence of a device (See Column 5 Lines 38-42 of Cepulis); provide the information to the computer system faster upon startup (See Column 5 Lines 26-38 of Cepulis); and to provide the device of Chari with a means for determining if a device is present, since Chari does not specifically state how the information is obtained.

29. Claims 3, 9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chari and Cepulis as applied to Claims 2, 8, and 14 above, and further in view of the "PCI IRQ Routing Table Specification" from Microsoft Corporation ("Microsoft").

30. In reference to Claim 3, Chari and Cepulis teach the limitations as applied to Claim 2 above. Chari and Cepulis do not teach locating the routing table in a read-only memory in the computing device. Microsoft teaches locating the routing table in a ROM array (See Page 6 Paragraph 3).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari and Cepulis with the routing table located in a ROM array of Microsoft, resulting in the invention of Claim 3, in order to provide a system which allows a PCI to PCI bridge add-in card in which the IRQ routing table only needs to describe the routing of the bridge's INTn# lines to the PCI interrupt router, or a transparent PCI to PCI bridge in which the IRQ routing table must report the IRQ routing for all devices behind the bridge, even when they are not present. Each of these devices provide a means for expanding the PCI bus in which a static routing table in a ROM array would be referable to a dynamic routing table (See Page 6 Paragraph 7 and Page 7 Paragraphs 1-4 of Microsoft).

31. In reference to Claim 9, Chari and Cepulis teach the limitations as applied to Claim 8 above. Chari and Cepulis do not teach locating the routing table in a read-only memory in the computing device. Microsoft teaches locating the routing table in a ROM array (See Page 6 Paragraph 3).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari and Cepulis with the routing table located in a ROM array of Microsoft, resulting in the invention of Claim 9, in order to provide a system which allows a PCI to PCI bridge add-in card in which the IRQ routing table only needs to describe the routing of the bridge's INTn# lines to the PCI interrupt router, or a transparent PCI to PCI bridge in which the IRQ routing table must report the IRQ routing for all devices behind the bridge, even when they are not present. Each of these devices provide a means for expanding the PCI bus in which a static routing table in a ROM array would be referable to a dynamic routing table (See Page 6 Paragraph 7 and Page 7 Paragraphs 1-4 of Microsoft).

32. In reference to Claim 15, Chari and Cepulis teach the limitations as applied to Claim 14 above. Chari and Cepulis do not teach locating the routing table in a read-only memory in the computing device. Microsoft teaches locating the routing table in a ROM array (See Page 6 Paragraph 3).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari and Cepulis with the routing table located in a ROM array of Microsoft, resulting in the invention of Claim 15, in order to provide a system which allows a PCI to PCI bridge add-in card in which the IRQ routing table only needs to describe the routing of the bridge's INTn# lines to the PCI interrupt router, or a transparent PCI to PCI bridge in which the IRQ routing table must report the IRQ routing for all devices behind the bridge, even when they are not present. Each of these devices provide a means for expanding the PCI bus in which a static routing table in a

ROM array would be preferable to a dynamic routing table (See Page 6 Paragraph 7 and Page 7 Paragraphs 1-4 of Microsoft).

33. Claims 4, 10, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chari as applied to Claims 1, 7, and 13 above, and further in view of US Patent Number 6,269,417 to Mahalingam ("Mahalingam").

34. In reference to Claim 4, Chari teaches the limitations as applied to Claim 1 above. Chari does not teach identifying at least one PCI device coupled to a PCI bus comprises identifying a bus number and a device number for each PCI device coupled to the PCI bus. Mahalingam teaches using a bus number and a device number to calculate a unique number identifying a PCI device (See Figure 1 and Column 2 Lines 40-51).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the method for identifying and numbering a PCI device of Mahalingam, resulting in the invention of Claim 4, in order to provide the device of Chari with a means for obtaining its slot and device information, since Chari does not specifically state how the information is obtained and since Chari incorporates by reference the method of Mahalingam (See Appendix A of Chari).

35. In reference to Claim 10, Chari teaches the limitations as applied to Claim 7 above. Chari does not teach identifying at least one PCI device coupled to a PCI bus

comprises identifying a bus number and a device number for each PCI device coupled to the PCI bus. Mahalingam teaches using a bus number and a device number to calculate a unique number identifying a PCI device (See Figure 1 and Column 2 Lines 40-51).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the method for identifying and numbering a PCI device of Mahalingam, resulting in the invention of Claim 10, in order to provide the device of Chari with a means for obtaining its slot and device information, since Chari does not specifically state how the information is obtained and since Chari incorporates by reference the method of Mahalingam (See Appendix A of Chari).

36. In reference to Claim 16, Chari teaches the limitations as applied to Claim 13 above. Chari does not teach identifying at least one PCI device coupled to a PCI bus comprises identifying a bus number and a device number for each PCI device coupled to the PCI bus. Mahalingam teaches using a bus number and a device number to calculate a unique number identifying a PCI device (See Figure 1 and Column 2 Lines 40-51).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the method for identifying and numbering a PCI device of Mahalingam, resulting in the invention of Claim 16, in order to provide the device of Chari with a means for obtaining its slot and device information, since Chari does not

specifically state how the information is obtained and since Chari incorporates by reference the method of Mahalingam (See Appendix A of Chari).

37. Claims 19, 20, 21, 26, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Chari and Cepulis.

38. In reference to Claim 19, Chari teaches that the adapter card slots are designed to receive PCI cards (See Column 6 Lines 49-59), which are inherently connected to the card slots through a PCI bus; identifying a bus number and a device number for at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Figure 34 and Column 6 Lines 49-59); and identifying an unoccupied PCI slot (See Figure 34). Chari does not teach locating a PCI IRQ Routing Table; identifying at least a bus number and a device number for each of a plurality of PCI slots using the routing table; and comparing the bus number and the device number for each of the identified PCI slots to the bus number and the device number of at least one of the PCI devices. Cepulis teaches the use of a PCI Interrupt Request Routing Table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7); and comparing the PCI IRQ Routing Table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use and comparison of

Cepulis, resulting in the invention of Claim 19, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

39. In reference to Claim 20, Chari teaches that the adapter card slots are designed to receive PCI cards (See Column 6 Lines 49-59), which are inherently connected to the card slots through a PCI bus; identifying a bus number and a device number for at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Figure 34 and Column 6 Lines 49-59); and identifying an unoccupied PCI slot (See Figure 34). Chari further teaches an apparatus in which the method is an application run on a computer system (See Figures 1, 4, and 7, Column 2 Lines 54-67, and Column 3 Lines 1-9 of Chari), and therefore inherently includes software encoded on a computer readable medium. Chari does not teach locating a PCI IRQ Routing Table; identifying at least a bus number and a device number for each of a plurality of PCI slots using the routing table; and comparing the bus number and the device number for each of the identified PCI slots to the bus number and the device number of at least one of the PCI devices. Cepulis teaches the use of a PCI Interrupt Request Routing Table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7); and comparing the PCI IRQ Routing Table Information for each PCI device slot (See

Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use and comparison of Cepulis, resulting in the invention of Claim 20, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

40. In reference to Claim 21, Chari teaches that the adapter card slots are designed to receive PCI cards (See Column 6 Lines 49-59), which are inherently connected to the card slots through a PCI bus; a memory that is inherently part of the computer system (See Figure 1 and Column 6 Lines 35-48) and operable to store information identifying a plurality of slots in the computing device (See Figure 34); and a processor coupled to the memory (See Figure 1 and Column 6 Lines 35-48) and operable to identify at least one PCI device coupled to a PCI bus coupled to the PCI slot (See Figure 34), and identify an unoccupied PCI slot (See Figure 34). Chari does not teach that the memory contains a PCI IRQ routing table; and the processor locating the routing table in the memory, identifying a bus number and a device number for each of a plurality of PCI

slots using the routing table, and comparing the bus number and the device number for each of the plurality of identified PCI slots to the bus number and the device number of the at least one PCI device. Cepulis teaches the use of a PCI Interrupt Request Routing Table to track PCI bus, device, and slot numbers for each PCI device slot (See Column 6 Lines 3-7); and comparing the PCI IRQ Routing Table Information for each PCI device slot (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the PCI Interrupt Request Routing Table use and comparison of Cepulis, resulting in the invention of Claim 21, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

41. In reference to Claim 26, Chari teaches generating a list of identified PCI slots associated with the computing device (See Figures 32, 33, and 34); and identifying an unoccupied PCI slot (See Figure 34). Because information pertaining to the slots is provided by the computer system, no physical inspection of the slots is required. Chari does not teach generating a list of one or more PCI devices coupled to the PCI bus

coupled to the PCI slot; and identifying an unoccupied PCI slot by comparing the list of PCI slots associated with the computing device with the list of one or more PCI devices coupled to the PCI bus. Cepulis teaches an NVRAM data structure that stores the information about each PCI device in the computer system (analogous to generating a list of one or more PCI devices coupled to the PCI bus) (See Column 5 Lines 54-61); and comparing the PCI IRQ Routing Table Information for each PCI device slot (analogous to the list of PCI slots) (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the NVRAM data structure use and comparison of Cepulis, resulting in the invention of Claim 26, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

42. In reference to Claim 27, Chari teaches generating a list of identified PCI slots associated with the computing device (analogous to an identification table identifying a plurality of PCI slots) (See Figures 32, 33, and 34); and identifying an unoccupied PCI slot (See Figure 34). Because information pertaining to the slots is provided by the

computer system, no physical inspection of the slots is required. Chari does not teach generating an enumeration table enumerating one or more PCI devices coupled to the PCI bus coupled to the PCI slot); and identifying an unoccupied PCI slot by comparing the identification table and the enumeration table. Cepulis teaches an NVRAM data structure that stores the information about each PCI device in the computer system (analogous to generating an identification table identifying a plurality of PCI slots) (See Column 5 Lines 54-61); and comparing the PCI IRQ Routing Table Information for each PCI device slot (analogous to the enumeration table) (See Column 6 Lines 3-5) with the NVRAM data structure storing the information about each PCI device in the computer system (See Column 5 Lines 54-61) (See Column 6 Lines 26-28).

One of ordinary skill in the art at the time the invention was made would combine the device of Chari with the NVRAM data structure use and comparison of Cepulis, resulting in the invention of Claim 27, in order to provide a system which uses the most accurate copy of the bus, device, and slot numbers, since the table was loaded at startup and thus will reflect the most up to date configuration information of the system (See Column 6 Lines 11-13 of Cepulis), as well as to provide the device of Chari with a means for determining availability of a slot, since Chari does not specifically state how the information is obtained.

Response to Arguments

43. Applicant's arguments filed 2 December 2003 in response to the rejections of Claims 1, 6, 7, 12, 13, and 18 have been fully considered but they are not persuasive.

Applicants have argued that Chari does not teach all of the limitations of Claims 1, 6, 7, 12, 13, and 18. However, as shown in the rejections above, Chari does teach all of the limitations of the aforementioned claims.

Applicants have further argued that "it is assumed that all eight slots in slot group number one are occupied or were occupied at least at some time" (Page 14 Lines 1-2). Chari teaches determining whether an adapter is present or absent from a slot, but provides no basis for an assumption that adapters that are absent were present at one time (See Figure 34). Further, Claims 1, 6, 7, 12, 13, and 18 do not include a limitation that unoccupied PCI slots were not previously occupied.

Applicants have further argued that "Chari does not disclose any way of even determining whether a device is currently connected. Chari merely discloses displaying information that identifies a particular device that is or once was connected to the slot." (See Page 14 Lines 9-11). However, in order to provide information identifying a particular device, the device of Chari must inherently determine whether a device is currently connected. Therefore, the device of Chari knows which slots are unoccupied. Further, Chari shows that retrieving information about devices connected to or absent from a slot was known in the art.

44. Applicant's arguments filed 2 December 2003 in response to the rejections of Claims 2, 5, 8, 11, 14, and 17 have been fully considered but they are not persuasive.

Applicants have argued that Chari and Cepulis do not teach all of the limitations of Claims 2, 5, 8, 11, 14, and 17. However, as shown in the rejections above, Chari and Cepulis do teach all of the limitations of the aforementioned claims.

Applicants have further argued that Cepulis "merely discloses comparing two stored versions of the PCI device numbers and bus numbers to determine whether a PCI device has a new bus number that needs to be updated" (See Page 16 Lines 20-22). However, Cepulis states that the IRQ routing table contains "IRQ routing for each PCI device slot" (See Column 6 Lines 3-7). Because the information contained in the IRQ routing table pertains to the device slot, Cepulis can be used to teach the limitations not taught by Chari.

45. Applicant's arguments filed 2 December 2003 with respect to Claims 19, 20, and 21 have been fully considered but are moot in view of the new ground(s) of rejection. Applicant has modified the scope of the claims to include: "each of a plurality of PCI slots" replacing "at least one PCI slot"; "at least one PCI device" replacing "any PCI devices"; and "for each of the" replacing "of at least one of the". As shown above, such changes are not persuasive to overcome a rejection based on 35 USC §103. The new ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

Conclusion

46. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (8-5:30), Alt. Fridays (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5631.

tjc

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